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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,048	04/08/2004	Sadanand V. Deshpande	FIS920030397US1	3047

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EXAMINER	
INGHAM, JOHN C	
ART UNIT	PAPER NUMBER
2814	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/709,048	DESHPANDE ET AL.	
	Examiner	Art Unit	
	JOHN C. INGHAM	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,6-9,12-14 and 26-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,6-9,12-14 and 26-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 31 October 2007 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims **1-2, 6-9, 12-14 and 26-36** are rejected under 35 U.S.C. 103(a) as being unpatentable over Luning (US 6,506,642) and Fulford (US 6,258,680).

4. Regarding claims **1-2, 6-9, 12-14, 30-33 and 35**, Luning discloses in Figure 6 an integrated circuit structure comprising: a substrate (40); first-type transistors (left side nFET) on said substrate, wherein said first-type transistors comprise first gate conductors (41) and first spacers (60) adjacent said first gate conductors; second-type transistors (right side pFET) on said substrate, wherein said second-type transistors

comprise second gate conductors (42), said first spacers (44) adjacent said second gate conductors, said first spacers adjacent said second gate conductors and second spacers (60); first-type (N type) source/drain impurity implants (61) in areas of said substrate completely outside of and adjacent to said first spacers of said first gate conductors, wherein said first-type impurity implants are single and non-stepped; second-type (P type) source/drain impurity implants (62) in areas of said substrate completely outside of and adjacent to said second spacers of said second gate conductors, wherein said second-type impurity implants are single and non-stepped, wherein said first type impurity is spaced closer to said first gate conductors than said second type impurity is spaced from said second gate conductors; first silicide regions (64) proximate said first spacers of first-type transistors; and second silicide regions (63) proximate said second spacers of said second-type transistors, wherein said second silicide regions are farther from said second gate conductors than said first silicide regions are from said first gate conductors (W3 greater than W2).

Luning does not disclose: an oxide layer, wherein said oxide layer is on said first gate conductors and said second gate conductors, wherein said first spacers are on said oxide layer; an etch stop layer on said first spacers of the second-type transistor, and second spacers on said etch stop layer, wherein said etch stop layer is only on said first spacers that are adjacent said second gate conductors and said etch stop layer is not on said first spacers that are adjacent said first gate conductors, wherein said etch stop layer is between bottom surface of said second spacers and said oxide layers; wherein said second spacers are only on said etch stop layer on said first spacers that

are adjacent said second gate conductors, and said second spacers are not adjacent said first spacers that are adjacent said first gate conductors. Instead Luning shows that the double spacer is only on the second-type transistor, with no etch stop layer between the double spacer.

Fulford teaches in Fig 12 that an oxide liner is formed on a transistor gate conductor and also as a liner between nitride spacers, to act as an etch stop so that the spacers can be formed and removed separately (col 8 ln 17-22). The etch stop may be removed (item 150 as shown in Fig 13) from the horizontal surfaces, or may obviously be left on the horizontal surfaces (col 8 ln 51-54). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Fulford on the device of Luning so that the nitride spacers could be formed and removed separately from the underlying oxides. As explained by Luning, the etch stop may or may not be removed from horizontal surfaces, depending on what is desired. If the etch stop is not removed, the etch stop layer (Fig 13 item 150) will remain between bottom surfaces of the second spacer (Fig 13 item 162) and the oxide layer (Fig 13 item 128).

5. Regarding claims **26-29**, Luning discloses in Figure 6 an integrated circuit structure comprising: a substrate (40); first-type transistors (left side nFET) on said substrate, wherein said first-type transistors comprise first gate conductors (41) and first spacers (60) adjacent said first gate conductors; second-type transistors (right side pFET) on said substrate, wherein said second-type transistors comprise second gate conductors (42), said first spacers (44) adjacent said second gate conductors, said first

spacers adjacent said second gate conductors and second spacers (60); first-type (N type) source/drain impurity implants (61) in areas of said substrate completely outside of and adjacent to said first spacers of said first gate conductors; second-type (P type) source/drain impurity implants (62) in areas of said substrate completely outside of and adjacent to said second spacers of said second gate conductors, wherein said first type impurity is spaced closer to said first gate conductors than said second type impurity is spaced from said second gate conductors; first silicide regions (64) proximate said first spacers of first-type transistors; and second silicide regions (63) proximate said second spacers of said second-type transistors, wherein said second silicide regions are farther from said second gate conductors than said first silicide regions are from said first gate conductors (W3 greater than W2).

Luning does not disclose an oxide layer on said first gate conductors and said second gate conductors, wherein said first spacers are on said oxide layer and wherein said etch stop layer is between bottom surface of said second spacers and said oxide layer, or an etch stop layer on said first spacers of the second-type transistor, and second spacers on said etch stop layer, wherein said etch stop layer is only on said first spacers that are adjacent said second gate conductors and said etch stop layer is not on said first spacers that are adjacent said first gate conductors; wherein said second spacers are only on said etch stop layer on said first spacers that are adjacent said second gate conductors, and said second spacers are not adjacent said first spacers that are adjacent said first gate conductors.

Instead Luning shows that a double spacer (of nitride) is only on the second-type transistor, with no etch stop layer between the double spacer.

Fulford teaches in Fig 12 that an oxide liner is formed on a transistor gate conductor and also as a liner between nitride spacers, to act as an etch stop so that the spacers can be formed and removed separately (col 8 ln 17-22). The etch stop may be removed (item 150 as shown in Fig 13) from the horizontal surfaces, or may obviously be left on the horizontal surfaces (col 8 ln 51-54). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Fulford on the device of Luning so that the nitride spacers could be formed and removed separately from the underlying oxides. As explained by Luning, the etch stop may or may not be removed from horizontal surfaces, depending on what is desired. If the etch stop is not removed, the etch stop layer (Fig 13 item 150) will remain between bottom surfaces of the second spacer (Fig 13 item 162) and the oxide layer (Fig 13 item 128).

6. Regarding claim **34**, Fulford teaches that an oxide liner is formed on a transistor gate conductor and also as an etch stop layer between first and second nitride spacers so that the spacers can be formed and removed separately (col 8 ln 17-22).

7. Regarding claim **36**, Luning discloses the circuit structure of claim 26, wherein said first type impurity implants (Fig 6 item 61) are single and non-stepped, and wherein said second type impurity implants (Fig 6 item 62) are single and non-stepped.

Response to Arguments

8. Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection. However, the argument on page 9 that Fulford teaches away from claimed features is not persuasive because Fulford is not used to teach implant regions. Fulford teaches an oxide liner and etch stop layer between nitride spacers. Regarding the argument on page 9 that Fulford does not teach wherein said etch stop layer is between bottom surface of said second spacers and said oxide layers, Fulford recites that "*If desired*, an etch may be used to remove the oxide from horizontal surfaces. Resulting from deposition and *possible* etch, oxide layer.." It is therefore obvious that the etch stop layer may not be removed if so desired, and therefore will be between the bottom surface of the second spacers and the oxide layer. Finally, it is noted that although the instant Figures seem to show a single impurity implant, paragraph 07 of the instant specification recites that extension impurities (LDD regions) can be implanted adjacent the gate conductors.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHN C. INGHAM whose telephone number is (571)272-8793. The examiner can normally be reached on M-F, 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Howard Weiss/
Primary Examiner
Art Unit 2814

John C Ingham
Examiner
Art Unit 2814

/J. C. I./